**The Semiconductor Industry Transformation:**
**Key Commercial, Operational, and Legal Issues**

We are about to experience a generational shift in the semiconductor industry driven by the repatriation of semiconductor manufacturing to the US and Europe. The US has allocated over $50B as part of the Creating Helpful Incentives to Produce Semiconductors (CHIPS) Act. Between the European chips act and budget allocated by individual European countries, Europe is planning to allocate a similar amount in the next few years. Individual companies are also planning to invest heavily in their US and European manufacturing facilities. In the end, considering the enormous expense of building foundries with leading edge process nodes, we could expect this effort to take 5-10 years and to cost an order of magnitude more than currently allocated.

In anticipation of the upcoming surge in transactions in the semiconductor industry, it is important to ensure that the legal industry is up to speed and can move efficiently to support these efforts. IP, commercial, operational, business and logistical issues are particularly complicated in the semiconductor space, and it is in everyone's interest to have sophisticated and knowledgeable lawyers on both sides of each transaction.

With that in mind, here is a table that summarizes the main steps in the semiconductor chain from a product commercialization perspective and identifies various legal, business and operational issues to be considered. There are other ways to look at the semiconductor industry (e.g., tracking a semiconductor chip from the silicon and wafer stage to system integration and applications), and we will do that in future articles.

1. Chip concept and design planning.
    a. Activities/Services: Chip concept development and architecture design; modeling and simulation to validate the high-level blueprint of the chip; business and market analysis; competitive analysis; commercialization and revenue projections; research and development (R&D); file patents to establish both offensive and defensive layers around the technology.
    b. Equipment/Technologies: Computer-Aided Design (CAD) tools.
    c. Legal Agreements: Contractor/service agreements with vendors, joint development agreements (JDAs) with business partners, cost sharing and commercialization arrangements to divest risk.
    d. Commercial, Operational and Legal Issues: Confidentiality, IP rights ownership, revenue sharing, responsibilities, design complexity, cost optimization, and time-to-market

2. Chip and system design integration and IP/block licensing
    a. Activities/Services: License and integrate into chip design any relevant third-party IP blocks (e.g., processor cores, memory blocks, and interface protocols) to accelerate the design process and reduce costs; identify and license any relevant Special Interest Group (SIGs) and Standards technologies and patents to clear path for commercialization.
    b. Equipment/Technologies: Hardware Description Language (HDL) tools.
    c. Legal Agreements: Contractor/service agreements with vendors, joint development agreements (JDAs) with business partners, cost sharing and commercialization arrangements to divest risk, IP license agreements with key third party vendors of IP block/core technologies, agreements to join SIGs and Standard bodies, and to license relevant technologies.
    d. Commercial, Operational and Legal Issues: Scope of licenses, sublicensing, IP rights ownership, support services, warranties, indemnities, liability limitations, termination provisions, technology compatibility, integration challenges, cost optimization

3. Chip design and simulation
    a. Activities/Services: Engage external design services or consulting firms to assist in the chip design process.
    b. Equipment/Technologies: CAD tools, HDL tools, project management tools.
    c. Legal Agreements: Contractor/service agreements with vendors, joint development agreements (JDAs) with business partners, cost sharing and commercialization arrangements to divest risk.
    d. Commercial, Operational and Legal Issues: Scope of work, deliverables, payment terms, IP rights ownership, warranties, indemnities, design expertise, resource availability, project management, cost optimization

4. Foundry and manufacturing
    a. Activities/Services: Engage semiconductor foundries to manufacture chip designs based on the finalized design files and specifications.
    b. Equipment/Technologies: Lithography equipment, etching equipment, deposition equipment, cleaning equipment, other semiconductor manufacturing equipment deployed in fabs.
    c. Legal Agreements: Foundry agreements, contractor/service agreements.
    d. Commercial, Operational and Legal Issues: Process technology and technology node selection, capacity allocation, pricing, payment terms, quality assurance, warranties, liability, IP rights ownership, yield optimization, cost management, lead times, liquidated damages, incentive payments.

5. Testing
    a. Activities/Services: Test the manufactured chips for functionality, performance, and reliability.
    b. Equipment/Technologies: Inspection equipment, metrology equipment, automated test equipment (ATE)
    c. Legal Agreements: Assembly and test services agreements, contractor/service agreements with vendors involved in the testing process.
    d. Commercial, Operational and Legal Issues: Scope of work, quality requirements, warranties, payment terms, IP rights ownership, test coverage, test time reduction, defect detection, and reliability assessment.

6. Packaging and assembly
    a. Activities/Services: Contract with third parties for packaging and assembly services for the manufactured chips.
    b. Equipment/Technologies: Die bonding equipment, wire bonding equipment, pick-and-place machines, other equipment used for chip packaging and assembly.
    c. Legal Agreements: Assembly and test services agreements, contractor/service agreements with vendors involved in the packaging and assembly process.
    d. Commercial, Operational and Legal Issues: Scope of work, quality requirements, payment terms, IP rights ownership, packaging technology selection, thermal management, form factor optimization, and cost reduction.

7. Marketing, sales and distribution
    a. Activities/Services: Implement commercialization and channel strategy, marketing, engage resellers and distributors to sell the manufactured chips, direct agreements with OEMs, ODMs and system integrators, vertical integration within the chip vendor's own systems.
    b. Equipment/Technologies: None (this is a business execution phase that focuses on generating and executing on market demand).

c. Legal Agreements: Channel agreements (e.g., reseller and distributor agreements), master supply agreements / master purchase agreements, referral/lead generation agreements to drive sales.
d. Commercial, Operational and Legal Issues: Sales territories, pricing, payment terms, marketing support, warranty claims, inventory management, supply buffers, demand forecasting, customer support, channel management, warranties, indemnification, liability